ELLIOTT

mobile computing division

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MCS 920M computer

PROVISIONAL SPECIFICATION

February 1967

MCS 920M COMPUTER

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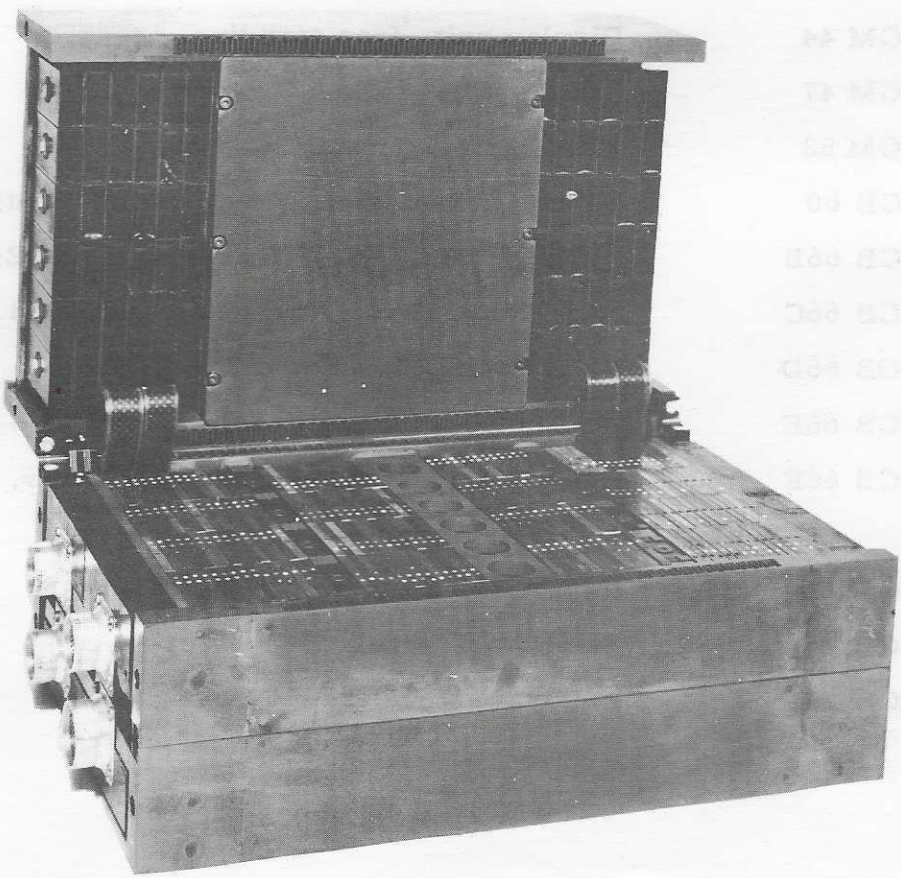
Contents

MCS 920M COMPUTER

RANGE OF COMPATIBLE SYSTEM UNITS

Catalogue No.	
MCM 2	Central Processor, 8192 words internal store.
MCM 21	Computer power supply, 20V DC input.
MCB 23	Primary power supply, 100-250V AC input.
MCM 24	Computer power supply, 240V 50 c/s input.
MCB 29	Primary power supply, 115V 400 c/s input.
MCB 30	Paper tape power supply, 100-250V AC input.
MCM 38	Mains filter 400 c/s.
MCM 39	Mains filter 50 c/s.
MCM 40	Control unit, 19in rack mounting.
MCM 41	Control unit, free standing.
MCM 43	Display unit, 19in rack mounting.
MCM 44	Display unit, free standing.
MCM 47	Additional 8192 words store.
MCM 52	Marginal test unit.
MCB 60	Paper tape controller 19in rack mounting.
MCB 66B	Paper tape reader and assoc. logic, 250 ch/s
MCB 66C	Paper tape reader and assoc. logic, 110 ch/s
MCB 66D	Teleprinter, stand and assoc. logic.
MCB 66E	On line adaptor for paper tape equipment.
MCB 66F	Paper tape and teleprinter controller, 19in rack mounting.
MCM 70	Paper tape reader, 250 ch/s
MCB 74	Paper tape punch, 110 ch/s
MCB 76	Paper tape punch, 110 ch/s (for use with MCB 66C only).



The MCS 920M COMPUTER Fig. 1

1. SUMMARY OF PRINCIPAL FEATURES

1.1 Introduction

An MCS 920M system consists of a variable number of units depending on the size of store and input-output capability required. The range of units available is as follows:-

(i) Computer, including 8192 words 5 μs Store.

(ii) Additional Store Units.

(iii) Power Units.

(iv) Control, Display and Marginal Test Units.

(v) Teleprinter and paper tape input and output equipment.

1.2 Computer Construction

(i) Construction in general conforms to ARINC 404 and DEF-133 Section A2.

(ii) The basic Computer pack including 8192 Word Store (MCM 2) is housed in a 3/4 short ATR case. Maximum weight 30.1 lb. (13.6 Kg)

1.3 Processor

Word length: 18 bits.

Number format: binary.

Instruction format: 1 instruction per word, single address.

Instruction code: 23 functions.

Store addressable: 65,536 words.

Instruction modification: the address portion may be modified.

1.4 Store

Type: coincident current ferrite core matrix.

Unit size: 8192 words.

Cycle time: 5μs

Maximum number: 7 additional, giving total capacity of 65,536 words.

1.5 Performance

Add: 19μs (unmodified)

Jump: 19μs (unmodified)

Multiply: 38μs (unmodified)

1.6 Programming Aids

(i) Built-in permanent initial instructions.

(ii) Symbolic Input Routine.

(iii) TRACE

(iv) ALGOL Compiler.

(v) FORTRAN Compiler.

1.7 Peripheral Interface

1. One outlet for paper tape equipment

   (i) mode: parallel.

   (ii) width: 8 bits.

   (iii) No. units: 1 controller for tape reader and tape punch or tape readers, tape punch and teleprinter.

   (iv) rate: 1 character/20μs

2. One outlet for up to 2048 input peripherals and up to 2048 output peripherals.

   (i) mode: parallel.

   (ii) width: 18 bits.

   (iii) multiplexing: external.

   (iv) rate: 1 word/20μs

   Block transfers at 1 word/10μs

2. THE PROCESSOR

2.1 Word Format

In the computer each word of information consists of an 18 digit binary number which may represent either a computer instruction or an operand of an instruction.

In the arithmetic functions of addition, subtraction, multiplication and division, the absolute value attributed to each digit of the word is:

18	17	16	15	.. ..	4	3	2	1
b	b	b	b		b	b	b	b
	-1	-2	-3		-14	-15	-16	-17
-1	$+2$	$+2$	$+2$	.. ..	$+2$	$+2$	$+2$	$+2$

The range of numbers that may be represented in the computer is from -1 to $+1-2^{-17}$.

When representing instructions, the 18 digits are divided into three numbers representing the modifier B in the function F and the address N, as follows:

b^{18}	b^{17}	b^{16}	b^{15}	b^{14}	b^{13}	b^{12}	b^{11}	b^{10}	..	b^{1}
1	2^3	2^2	2^1	2^0	2^{13}	2^{12}	2^{11}	2^{10}	..	2^0
B	F				N					

$B = 0/1$ $\quad 0 \leqslant F \leqslant 15$ $\quad 0 \leqslant N \leqslant 8191$

2.2 Registers

The registers which are addressed by the various functions are as follows:-

2.2.1 A Register:

This is an accumulator with a capacity of 18 digits which is used to hold the result of calculations prior to transfer to the store or output channel.

2.2.2 Q Register:

This is a register with a capacity of 18 digits which is used to hold information temporarily during a computation and also as an extension of the accumulator for numbers containing more than 18 significant digits. In this case it extends the less significant end of the accumulator by 17 digits, using digits 2 to 18 of the Q register. The register used in this way is known as the Auxiliary register.

2.2.3 B Register:

This 18 digit register holds the number which is added to the N digits of the instruction to form the address if the B digit of the instruction is a "one".

2.3 Program Levels and Interrupt Facility

2.3.1

Provision is made for four program priority levels, which are arranged to operate on an interrupt basis. If while the computer is running an interrupt signal is received for a higher level program, the program currently being obeyed will be temporarily suspended while the higher level program is obeyed. When this higher level program is terminated by a program terminate instruction the computer will revert to the lower level program and continue from the point at which it was interrupted.

2.3.2

A sequence control register (SCR) and a modification register (B register) are provided for each program level. These registers are held in the computer store in location 0 - 7 as follows:

	SCR	B Register
Program level 1	0	1
2	2	3
3	4	5
4	6	7

Program level 1 is the highest priority and cannot be interrupted.
Program level 2 may be interrupted only by level 1.
Program level 3 may be interrupted by levels 1 and 2.
Program level 4 may be interrupted by levels 1, 2 and 3.
Interruption occurs as a result of a signal received from a peripheral equipment.

2.4 Store Addressing

2.4.1

The store is divided into blocks of 8192 words each; numbers or instructions may be placed in any location of any available block. The N digits of an unmodified instruction specify a location of the block in which the instruction itself is located; i.e. the absolute address of the location is formed by adding the N digits to digits 14-16 of the Sequence Control Register, the latter digits being those which specify the block in which the instruction is located.

2.4.2

The address specified by an instruction may be modified by adding the contents of the B register to the unmodified address prior to implementing the instruction. This does not affect the instruction held in the store. Where the instruction is required to be modified, this is signified by a one in digit 18 position of the instruction. Only the least significant 16 bits of the sum will be used as the address: by this means the range of storage locations which may be specified by the computer instructions is increased to 65,536 words.

2.5 Instruction Code

In the following description N refers to the absolute address specified by an instruction, unmodified or modified, as described in 2.4 above.

Function Number	Title	Specification
0	Set B register	Place in the B register of the current program level, and in the Q register, the contents of the store location specified by N. The contents of A are not affected by this function.
1	Add	Add the contents of the store location specified by N to the accumulator. The contents of Q are not affected by this function.
2	Negate and Add	Negate the contents of the accumulator and add the contents of the store location specified by N. The contents of N are also placed in the Q register by this function.
3	Store Auxiliary Register	Place the most significant 17 bits of the Q register in the least significant 17 bits of the store location specified by N. The most significant bit of the store location is made zero. The contents of A are not affected by this function.
4	Read	Copy the contents of the store location specified by N into the accumulator.
5	Write	Copy the contents of the accumulator into the store location specified by N.
6	Collate	Place ones in the accumulator in only those digit positions in which both the contents of accumulator and of the store location specified by N are ones. (i.e. form in the accumulator the logical product of the contents of the accumulator and the store location specified by N).

Function Number	Title	Specification
7	Jump if zero	If the number in the accumulator is zero, place N in the sequence control register of the current program level. The contents of the accumulator are not affected by this function.
8	Jump	Place N in the sequence control register of the current program level. The contents of A and Q are not affected by this function.
9	Jump if negative	If the number in the accumulator is negative, place N in the sequence control register of the current program level. The contents of A are not affected by this function.
10	Count in store	Increment the contents of the store location specified by N by $+2^{-17}$. The contents of A and Q are not affected by this function.
11	Store SCR	Copy the contents of digits 1-13 of the sequence control register of the current program into the store location specified by N setting digits 14-16 of of this location to zero. Copy digits 14-16 of the sequence control register into the Q register, setting the remaining digits of Q to zero. The contents of the sequence control register, and of A, are not affected by this function.
12	Multiply	Multiply the number in the accumulator by the number in the store location specified by N, and place the result in the accumulator and the most significant 17 digit positions of the Q register.
13	Divide	Divide the number in the accumulator and the most significant 17 digits of the Q register by the number in the store location specified by N, and place the result in the accumulator making the least significant digit a one so that it is correctly rounded to 17 digits. The result is also placed in Q, but with the least significant digit a zero.

Function Number	Title	Specification
14	Shift and block transfer	Note that for function 14 only the 13 least significant bits of N are meaningful.
14a)	Left shift $0 \leqslant N \leqslant 36$	Shift the contents of the double-length number in A and Q left by the number of places specified by N (= multiply by 2n).
b)	Right shift $8156 \leqslant N \leqslant 8191$	Shift the contents of the double-length number in A and Q right by 8192-N places. (= divide by 2^{8192-n}).
c)	Block input $2048 \leqslant N \leqslant 4095$	Transfer n words of information from the device specified by bits 1-11 of N into store locations m to m+n-1. m is the contents of the accumulator and n is the contents of the Q register.
d)	Block output $4096 \leqslant N \leqslant 6143$	Transfer n words of information to the device specified by bits 1 to 11 of N from store locations m to m+n-1 where m is the contents of the accumulator and n is the contents of the Q register.
15	Miscellaneous	Note that for function 15 only the 13 least significant bits of N are meaningful.
a)	Input $0 \leqslant N \leqslant 2047$	Input to the accumulator one 18 bit word from the device specified by bits 1 to 11 of N.
b)	Output $4096 \leqslant N \leqslant 6143$	Output from the accumulator one 18 bit word to the device specified by bits 1 to 11 of N.
c)	Tape Reader Input N = 2048 Teleprinter Input N = 2052	Input one 8 digit character from the tape reader or teleprinter. Shift the previous contents of the accumulator left 7 places and place the input character in the least significant 8 digit positions of the accumulator.

Function Number	Title	Specification
15d)	Tape Punch Output N=6144 Teleprinter Output N=6148	Output the least significant 8 bits of the accumulator to the tape punch channel.
e)	Program Terminate N=7168	Terminate current program level.

2.6 Instruction Times

The following are typical instruction times in micro-seconds:

Function	Operation	Time un-modified	Time modified
0	Set B register	22	28
1	Add	19	25
2	Negate and Add	21	27
3	Store Aux Register	20	26
4	Read	19	25
5	Write	20	26
6	Collate	19	25
7	Jump if A zero(A = +ve)	17	23
	(A = -ve)	16	22
	Jump if A zero (A=0)	21	27
8	Jump	19	25
9	Jump if A negative ($A \geqslant 0$)	15	21
	Jump if A negative ($A < 0$)	19	25
10	Count in store	20	26
11	Store S register	25	31
12	Multiply	38	44
13	Divide	39	45
14	Shift (n places)	16+n	22+n
"	Block transfer (n words)	18+10n	24+10n
15	Input-output	20(min.)	26(min.)
"	Program terminate	20	26

2.7 Processor Construction

2.7.1

The processor is constructed out of monolithic integrated, 'diode transistor' logic circuits. The monolithic circuits are encapsulated in 'flat-packs : up to three flat-packs are mounted on a heat sink, together with etched nickel-mylar interconnecting film and 15 etched connection pins, to form a 'logic module' which is non-reparable. The size of the logic module is approximately $1\frac{1}{2}$in x 1in x .15in. For special purposes (e.g. external line drivers, timing circuits) discrete components are used in a module in conjunction with integrated circuits. All interconnections within a module are welded.

2.7.2

Interconnections between logic modules are accomplished by a number of layers of etched nickel-mylar film; at each module position the pins pass through the layers and are welded to 'tabs' which are formed by the ends of the nickel tracks when required. The module is inserted so that its interconnection pins are alongside the pins mentioned above; a wire-wrap joint is then made around each pair of pins thus making reliable electrical connection to the module while permitting it to be removed when replacement is necessary. Each row of modules is firmly clamped together to retain the modules in position and to enable heat to be dissipated evenly.

2.7.3

The processor contains four independent areas of multilayer film as described above, each being approximately 6in square. Connections between these are accomplished by short wire links, wrapped at each end or, where a hinge has to be crossed, by flexible film wire.

2.7.4

The processor requires a total of 399 modules of about 20 different types. Each area of interconnecting film accommodates four rows of 28 modules each.

2.8 Power Requirements

The processor operates from rails of +5.5V at 5A ± 10%, and and -5.5V at 0.5A ± 10%. The power dissipation does not exceed 30W.

3. STORE

3.1 The basic Computer has an integral store of 8192 words which may be increased in blocks of 8192 words by the addition of up to 7 additional stores, giving a maximum total capacity of 65,536 words.

3.2 Construction

The circuits associated with the core matrices are composed of discrete components welded on to etched nickel-mylar interconnecting film and encapsulated inside a metal heat sink 2" x 1" x .45" forming a 'circuit module' which is non-reparable. Modules containing integrated logic circuits, as described for the processor, are also used. Connections between modules and to the core matrix are made by multi-layer film similar to that in the processor. The additional stores have their own cable drivers and receivers and are connected to common Data Bus lines by plug and socket connectors.

The internal store has dummy modules in the driver and receiver positions, is connected to the processor by flexible wire film and forms part of the basic computer pack.

3.3 Store Power Requirements

The supplies needed for 1 store, internal or external, are as follows:-

+5.5 Volts 0.7A ± 10% (average)
-5.5 Volts 0.7A ± 10% "
+15 Volts 610mA ± 10% "
-15 Volts 30mA ± 10% "

The average dissipation is 20 watts and the maximum 30 watts. If more than one store is connected only one can be active at any one time, so the power requirements are not increased pro-rata.

The combined average dissipation for 2 units is 35W.

The combined maximum dissipation for 2 units is 45W.

4. POWER UNITS

4.1

The power supplies required by the basic computer and one additional store, or by two additional stores, can be obtained from a choice of power units, as follows:-

a) Power Unit MCM 21

A miniature, ruggedised power unit producing the required supplies from a primary DC input which can be in the range 20 to 42V. The unit is fully protected and in the event of the primary supply failing or going outside the above limits the outputs are sequenced off in such a way that store contents are retained.

b) Power Unit MCM 24

This unit produces the required supplies from an AC mains input of 100-125V or 200-250V ± 10%, 45-60 c/s. Protection or store retention facilities are not included.

4.2 Primary Supply Units

Primary power units to supply 24V DC are available as follows:-

a) Primary Power Supply MCB 23

Output 24V DC, input 100-125V or 200-250V, 50-60 c/s, Incorporating 2 A.H. nickel cadmium battery and charging equipment for 15 minutes emergency operation.

b) Primary Power Supply MCB 29

Output 24V DC input 115V, 400 c/s 3-phase. Incorporates 2 A.H. nickel cadmium battery and charging equipment for 15 minutes emergency operation.

5. CONTROL, MARGIN AND DISPLAY UNITS

5.1

These provide the following facilities:-

a) Word generator: a set of switches on which the binary digits of a word may be set up by operator or engineer. The word may be interpreted as a starting address, as an input, or as an instruction.

b) Operator's Controls: to provide sufficient facilities for program check-out and running.

c) Engineer's Controls: additional facilities for fault location, including marginal, voltage and timing checks.

d) Monitor lamps: to monitor the registers or control bistables within the processor, and various states of the computer.

e) On-Off switch

f) Master Control Switch: This switch, which is key operated, has three positions, namely: auto, operate and test. According to its position only the relevant control switches are enabled.

The processor can be used without a control panel connected, provided the program required has been previously loaded, in which case if the processor requires contents of word generator it will see 8:8177 (Jump to 8177).

For full specification of the 920M Control Unit (Catalogue No. MCM 40/41)see separate Specification 322/SM40/2.67/A.

6. PROGRAMMING AIDS

6.1 Initial Instructions

A set of permanently available initial instructions facilitates the reading of program tapes into the computer. These are obtained for 8192 word store computers by entering the same starting address which corresponds to the last 12 store locations. The initial instructions and their respective addresses are tabulated below:-

Address	Instruction			Effect
'N' digits	'B'	'F'	'N'	
8180	/	15	8189	(-3)
8181		0	8180	(Set B-Register to -3)
8182		4	8189	(Set Accumulator initially)
8183		15	2048	(Shift and input tape character)
8184		9	8186	(Jump to 8186 if Accumulator is negative)
8185		8	8183	(Jump to 8183 if Accumulator is positive)
8186		15	2048	(Shift and input final tape character of word)
8187	/	5	8180	(Store word read in)
8188		10	0001	(Count in B-Register)
8189		4	0001	(Read B-Register)
8190		9	8182	(Jump to 8182 if Accumulator is negative)
8191		8	8177	(Jump to 8177 if Accumulator is positive)

Notes:

When entered at 8181 the routine initially reads words into 8177, 8178 and 8179, control is then transferred to location 8177. If these instructions set the B Register to -n and then transfer control to 8182, words can then be read into the sequence of n locations ending at 8179.

Control is then transferred again to location 8177 so that a transfer instruction read into that location can trigger the program.

6.2 Symbolic Input Routine

SIR enables programs to be written in modified machine code form. Essential details of SIR are given below. Full details of SIR can be obtained from the SIR Handbook.

SIR Symbols used for the Major Facilities

(i)	Identifier		Group of up to six letters or numbers commencing with a letter.
(ii)	Constants		
	(a)	Integer or fraction	±
	(b)	Octal groups	&
	(c)	Alphanumeric Groups	£
(iii)	Addresses		
	(a)	Absolute	an unsigned integer
	(b)	Block relative address	N;
	(c)	SCR relative	;±N
	(d)	Identified address	Identifier ± Integer (if required)
	(e)	Literal address	Any constant as in (ii) above or = followed by an instruction (absolute address only).
(iv)	Skips		>+N
(v)	Comment		( ) e.g. (entry point)
(vi)	Option		*+N where N is the sum of the following:

1. Punch list labels.
2. Load and go operation (otherwise punch relocatable binary tape).
4. Clear the store up to the assembler.
8. Punch a binary loader tape.
16. Continue assembly at location 8.
32. Set dictionary below the program.

(vii) Patches ↑+N

(viii) End of SIR program %

When more than 1 tape is used only the last tape ends with %, the others end with 'stop code' on a new line.

Note: Every new line symbol must be followed by at least four blanks.

6.3 Trace Facility

The tracing of faults or errors in programs is simplified by use of the Trace Facility. The TRACE program is operated on program level 1 and the program under examination on program level 4. A repetitive interrupt signal is produced for level 1 and the timing of the interrupt logic is such that when program 1 terminates, a single instruction of level 4 program is obeyed before the computer returns to level 1. Thus the level 1 program is obeyed after each instruction of the level 4 program and is able to examine the effect of each level 4 instruction. The trace program may operate on any one of levels 1, 2 and 3 and may examine programs on any level lower than itself.

6.4 ALGOL Compiler

A compiler is available to enable programs written in ALGOL to be used.

6.5 FORTRAN Compiler

A compiler is also available to enable programs written in FORTRAN to be used.

7.0 PERIPHERAL INTERFACE

This specification describes the timing of the control and data waveforms between the computer and the peripherals and describes the circuits used within the computer to transmit and receive these waveforms. It also gives a schedule of pin connections for the various inter-connecting cables.

7.1 Timing

System outline:

(a) Input

When an input is required the computer sends a 'input select' signal to the specified peripheral for which a 'reply' must be received before data transfer can commence. Until such time the computer will wait. When input has taken place the 'input select' goes down indicating the finish of data transfer.

(b) Output

When an output is required the computer sends an 'output select' to the specified peripheral. The peripheral will 'reply' indicating that data transfer has taken place. Until such time the computer will wait. When output has taken place the input select goes down indicating the finish of data transfer.

7.2 Interface Signals

INPUT SELECT) OUTPUT SELECT)	From computer, one line each. These signals are normally in the false state; the appropriate signal is set to the true state to cause a word to be transferred.
INPUT REPLY) OUTPUT REPLY)	To computer, one line each. This is normally false: the signal is set true to indicate when, after the appropriate select signal has become true, output information has been accepted by the device or input information is available on the computer input lines. When the reply has been detected by the computer, the select signal will return to false and the reply must then also return to false.

ADDRESS	From computer. 11 parallel lines carry the address digits of the selected peripheral. These are set before the select signal goes true and will remain set for as long as either the select signal or block transfer signal remains true. The state of the lines otherwise is not defined and the changes in this state may occur at any time.
OUTPUT INFORMATION	From computer. 18 parallel lines carry the binary digits of the word to be output for as long as the select signal remains true. The state of the lines otherwise is not defined and changes in this state may occur at any time.
INPUT INFORMATION	To computer. 18 parallel lines carry the binary digits of a word to be input to the computer. They should be held in the correct state for as long as the REPLY and INPUT SELECT signals are both true. The lines should be in the "Zero" state while the INPUT SELECT signal is false and also when an input instruction occurs which does not address the particular device or devices being considered.
INTERRUPT 1 INTERRUPT 2 INTERRUPT 3	To computer. These signals, normally false, are made true to start action of the computer priority program numbers 1, 2 and 3 respectively. They must be held true for 6μs or until action of the corresponding programs is detected, which will occur only if no program of a higher level requires attention. They must be made false before the program concerned terminates.
RESET	Reset signifies to external devices when the computer is in the reset state. Reset goes true when the 'jump' button on the control unit is operated and also when the computer starts working after:- (a) The power supplies become correct (b) The store temperature becomes correct after being under temperature.

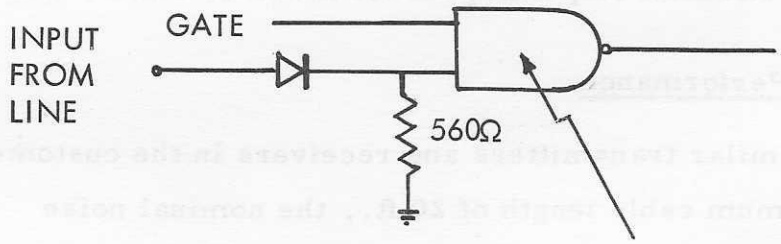
COMPUTER ON — From computer. +5V provides an indication that the computer power supplies are switch on.
(For timing diagrams see 7.6, Figs. 3 & 4)

7.3 Peripheral Line Driver and Receiver Circuits

The driver and receiver circuits described below are those contained within the 920M Computer, making direct connection with the lines of the peripheral channel. It is recommended that driver and receiver circuits within customers' peripheral equipment should be the same.

7.3.1 Line Receiver

The circuit below is used to receive signals from lines carrying information to the computer from peripheral equipment.



LOGIC ELEMENT D93059
(ONE OF THE ELLIOTT D9
FAMILY OF DTL LOGIC
BUILDING BLOCKS)

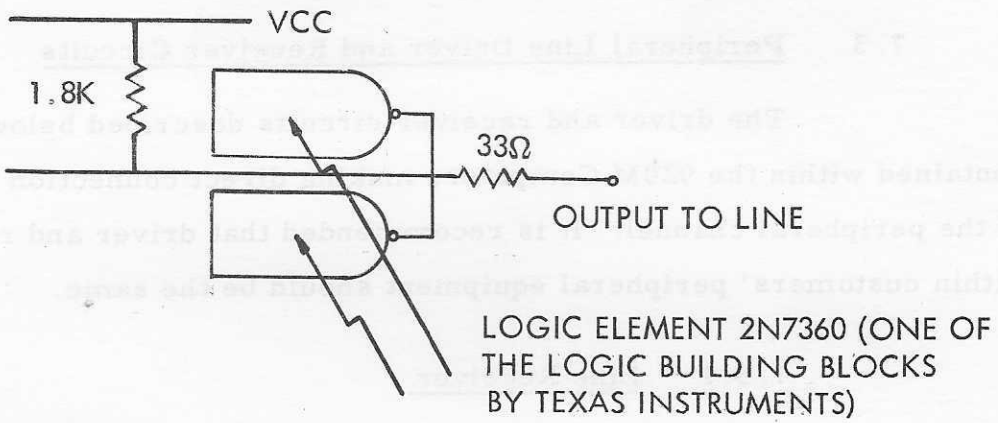
Nominal threshold: 2V at 25°c

Nominal "1" input level requirement : 3V at 4mA

Nominal "0" input level requirement : 0V at 0mA

7.3.2 Line Transmitter

The circuit below is used to drive lines from the computer to peripheral equipment:



Nominal "0" level output : 0.4V at 10mA Sink

Nominal "1" level output : 3.2V at 16mA Source

Nominal output impedance in either state : 50Ω

7.4 Cable Performance

With similar transmitters and receivers in the customer's equipment and a maximum cable length of 20 ft., the nominal noise margin of 1 volt will be maintained over the operational temperature range.

7.5 Inter-connection Details between system units are given in the following cable schedules:-

Power Unit-Computer Connections

Computer Plug A: Hellerman Deutsch - DS MOO-19-33PW

Socket required on Cable : " " DSMO7-19-33SW

Pin connections as below:-

Computer Plug Pin	Function	Computer Plug Pin	Function	Computer Plug Pin	Function
1	OV	28	-6V	59	Ov (for +6V (L)
2	OV	29	Store Temp.	60	HT+
3	OV		Ref.	61	HT+
4	OV	30	On SS	62	+15V
5	OV	31	Auto-Man SW	63	+15V
6	OV	32	Ov (for +15V)	64	+6V(L)
7	OV	33	+15V	65	+6V (L)
8	OV	34	+15V	66	+6V(L)
9	OV	35	Sense +15V	67	+6V (L)
10	OV	36	Slave On/Off	68	+6V (L)
11	OV	37	Store under	69	+6V (L)
12	Threshold		Temp.	70	+6V (L)
	Margin 1	38	Slave Volts	71	OV (for -6V)
13	OV (for +		Correct	72	Ov (for -6V)
	15V)	39	Ov to Margin	73	OV (for +15V)
14	+6V (S)		Test Box	74	OV (for +15V)
15	+6V (S)	40	+6V (L)	75	Ov (for +6V (L)
16	+6V (S)	41	+6V (L)	76	Drive Margin 2
17	Timing	42	+6V (L)	77	Threshold
	Margin 2	43	+6V (L)		Margin 2
18	Timing	44	+6V (L)	78	Strobe
	Margin 1	45	+6V (L)		Margin 2
19	+6V to Margin	46	+6V (L)	79	OV (for +6V (S)
	Test Box	47	Sense +6V	80	Ov (for +6V (S)
20	Strobe	48	OV (for +6V (L)	81	OV (for +6V (S)
	Margin 1	49	-15V	82	Mains Earth
21	Power Supp.	50	Sense -15V		
	Correct	51	HT-		
22	Drive	52	HT-		
	Margin 1	53	-6V		
23	+5V (Aux)	54	Store over Temp.		
24	OV (only used in	55	-6V		
	extra store				
	(for- 6V)	56	-6V Sense		

Com-puter Plug Pin	Function	Com-puter Plug Pin	Function
25	-5V Aux.	57	OV(for +5V Aux)
26	Off SS	58	OV(for -15V)
27	-6V to Margin Test Box		

Peripheral to Computer

Computer Plug C:- Hellerman Deutsch DSMOO-19-33 PX

Cable Socket required:- Hellerman Deutsch DSMO7-19-33SX

Pin connections as below:

Computer Plug Pin	Function	Computer Plug Pin	Function
1	OV	36	P1-8
2	OV	37	P1-3
3	OV	38	P1-11
4	OV	39	P1-14
5	Periph O/P3	40	P1-13
6	Periph O/P4	41	P1-15
7	Periph O/P2	42	P1-18
8	Periph O/P6	43	P1-17
9	Periph O/P1	44	P1-16
10	Periph O/P17	45	P1-6
11	Periph O/P15	46	P1-5
12	Periph O/P8	47	P1-4
13	Periph O/P5	48	+5V
14	Periph O/P18	49	Periph Add 1
15	Periph O/P16	50	Periph Add 5
16	Reset to Periph.	51	Periph Add 6
17	Per Add 11	52	Periph Add 7
18	Per Add 9	53	Periph O/P 11
19	Per Add 3	54	Periph O/P 14
20	Per Add 4	55	Periph Add 10
* 21	Interrupt 3	56	Periph Add 8
* 22	Interrupt 1	57	Periph O/P 9
* 23	Interrupt 2	58	Periph O/P 12
* 24	I/P Reply	59	Periph O/P 13
* 25	O/P Reply	60	Periph O/P 7
* 26	O/P Select	61	Periph O/P 10
* 27	I/P Select	62	OV
28	Per Add 2	63	OV

Computer Plug Pin	Function	Computer Plug Pin	Function
29	OV	64	INT 3 (from P/T)
30	P1-7	65	INT 1 (from P/T)
31	P1-9	66	INT 2 (from P/T)
32	P1-10	67	OV
33	P1-12	68	Block Transfer
34	P1-1	69	OV
35	P1-2	70-81	OV
		82	Mains earth

NOTE: 0 volts is connected internally to mains earth through 47 ohms.

Paper Tape Controller to Computer

Computer Socket H : Hellerman Deutsch DSMOO-19-33-SY

Cable Plug Required : Hellerman Deutsch DSMO7-19-33-PY

7.5.1 Cable construction

(i) All lines marked with an asterisk should be made in miniature coaxial cable with not more than 3 outers sharing one 0-volt pin.

(ii) All other lines can be made with 7/.0076" wire.

(iii) All lines should be enclosed within an outer braided screen which is used as the OV connection between computer and peripheral equipment.

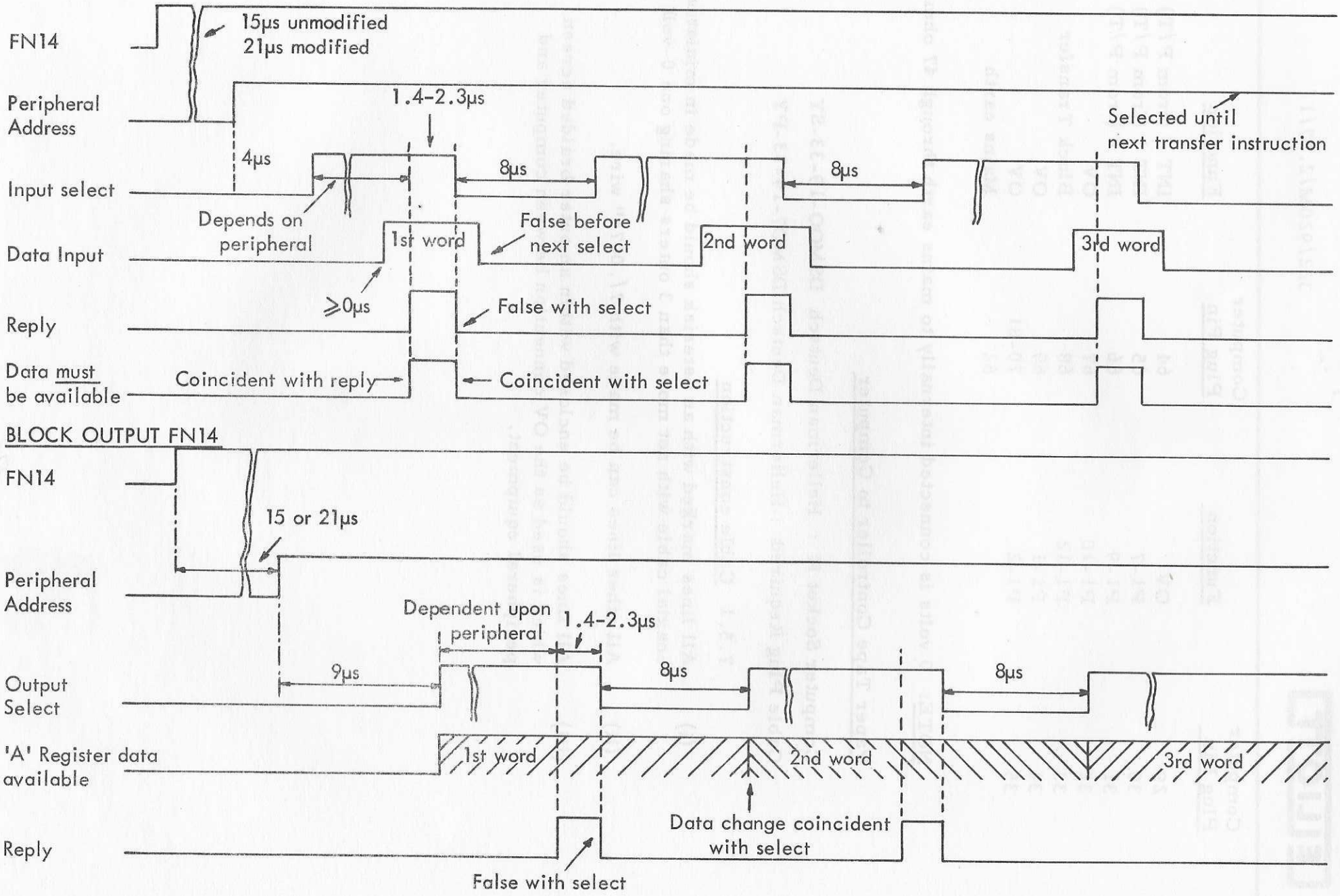
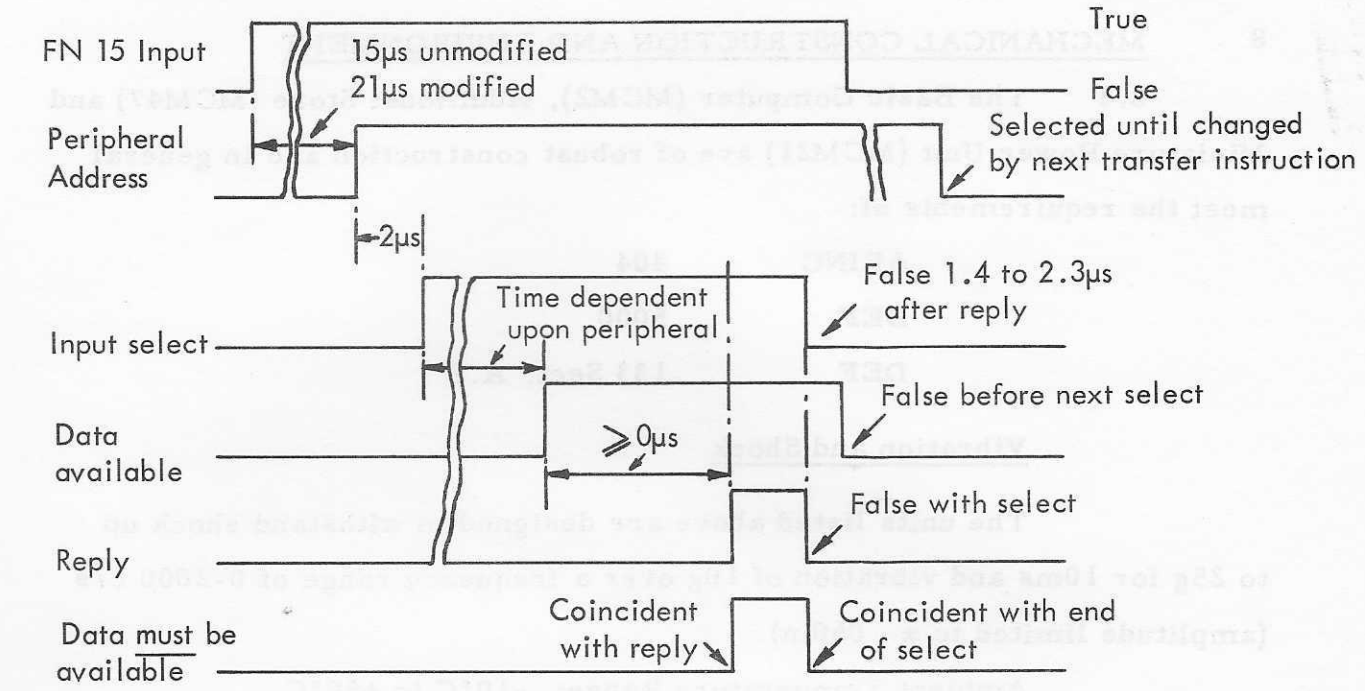
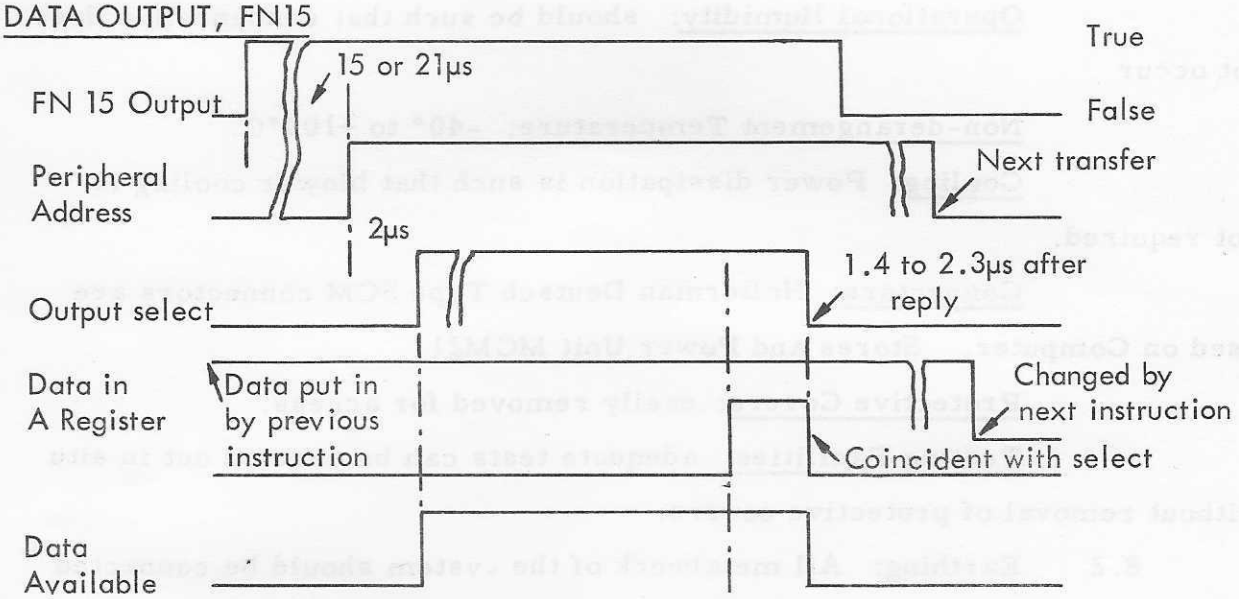

BLOCK INPUT FN14
FN14
15µs unmodified
21µs modified
Peripheral Address
1.4-2.3µs
Selected until next transfer instruction
4µs
8µs
8µs
Input select
Depends on peripheral
1st word
False before next select
2nd word
3rd word
Data Input
≥0µs
False with select
Reply
Data must be available
Coincident with reply
Coincident with select
BLOCK OUTPUT FN14
FN14
15 or 21µs
Peripheral Address
Dependent upon peripheral
1.4-2.3µs
9µs
8µs
8µs
Output Select
'A' Register data available
1st word
2nd word
3rd word
Data change coincident with select
Reply
False with select

Fig. 3

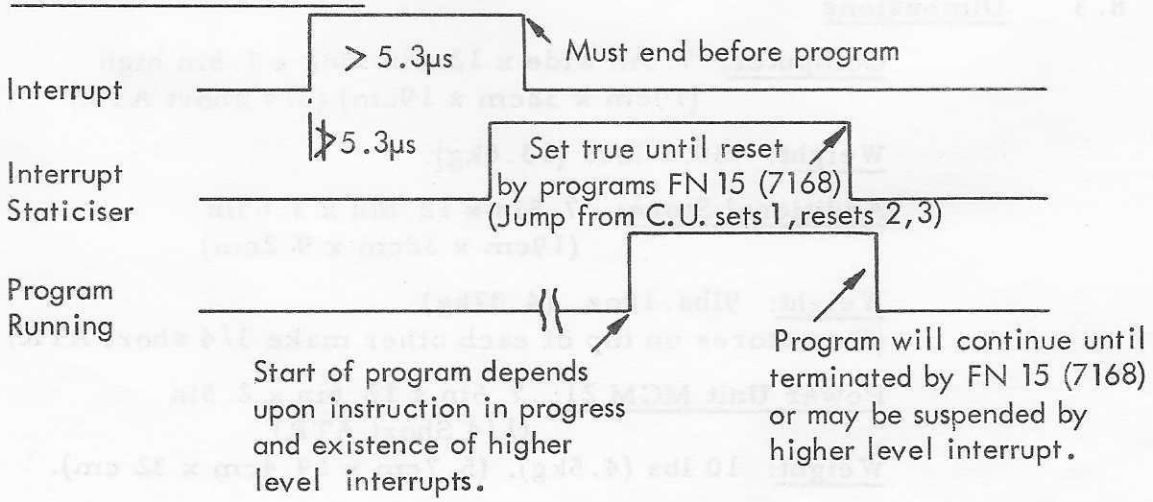
DATA INPUT, FN 15



DATA OUTPUT, FN15



PERIPHERAL INTERRUPTS



TIMING WAVEFORMS Fig. 4

8. MECHANICAL CONSTRUCTION AND ENVIRONMENT

8.1 The Basic Computer (MCM2), Additional Store (MCM47) and Miniature Power Unit (MCM21) are of robust construction and in general meet the requirements of:

ARINC	404
DEF	5000
DEF	133 Sect. A.2

Vibration and Shock

The units listed above are designed to withstand shock up to 25g for 10ms and vibration of 10g over a frequency range of 0-2000 c/s (amplitude limited to ± .060in).

Ambient Temperature Range: -10°C to +55°C.

Operational Humidity: should be such that condensation does not occur

Non-derangement Temperature: -40° to +100°C.

Cooling: Power dissipation is such that blower cooling is not required.

Connectors: Hellerman Deutsch Type SCM connectors are used on Computer, Stores and Power Unit MCM21.

Protective Covers: easily removed for access.

Testing Facilities: adequate tests can be carried out in situ without removal of protective covers.

8.2 Earthing: All metalwork of the system should be connected to mains earth. OV is connected to earth through 47 ohms.

8.3 Dimensions

Computer: 7.5in wide x 12.6in long x 7.5in high
(19cm x 32cm x 19cm) (3/4 short ATR)

Weight: 30.1 lbs. (13.6kg).

Additional Store: 7.5in x 12.6in x 3.65in
(19cm x 32cm x 9.2cm)

Weight: 9lbs.10oz. (4.37kg).
(Two stores on top of each other make 3/4 short ATR)

Power Unit MCM 21: 7.5in x 12.6in x 2.5in
(1/4 Short ATR)

Weight: 10 lbs (4.5kg). (5.7cm x 19.4cm x 32 cm).

9. ADDITIONAL SYSTEM UNITS

The following additional units are available for incorporation in any 920M Computer System:-

9.1 MCB 23: Primary Power Supply

Output: 24V D.C. for supply to Power Unit MCM 21

Input: 100-125V, 200-250V ± 50-60 c/s.

Temperature: -40°C to 55°C (Non-derangement -55°C to +100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sect. L.2 (As for computer)

Size: $16\frac{1}{2}$in x $6\frac{3}{4}$in x 12in (Weight: 54.5 lbs)
(14.9cm x 17.1cm x 30.5cm)

The unit includes 2.A.H. Nickel cadmium batteries for 15 minutes emergency operation.

9.2 MCM 24: Computer Power Supply

Input: 100-125V or 200-250V ± 10%, 50-60 c/s

Temperature: 0° to 50°C (Non-derangement, -40°C to +100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sec. L.1.

Size: 19in rack mounting x 7in high x 12in deep. (Weight: 45lb. approx.)

9.3 MCB 29: Primary Power Supply

Input: 115V, 400 c/s 3ph.

Output: 24V D.C. for supplying MCM 21.

Temperature: -40°to 55°C (Non-derangement -55°C to +100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sec. L.2

Size: $16\frac{1}{2}$in x $6\frac{3}{4}$in x 12in (Weight: $39\frac{1}{4}$ lb)

Includes emergency supply for 15 minutes by batteries.

9.4 MCB 30: Paper Tape Power Supply

Input: 100-125V, 200-250V, 50 c/s ± 1 c/s.

Output: All supplies for MCB60 Paper Tape Reader and Paper Tape Punch

Temperature: 0 to 50°C (Non-derangement -40°C to +100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sect. L.1.

Size: 19in Rack mounting x $8\frac{3}{4}$in high x 12in deep.
Weight: 66lb. approx.

9.5 MCM 38: Mains Filter

Frequency: 400 c/s.

Mounting: Rack. 19in x $5\frac{1}{4}$in x $3\frac{1}{2}$in

9.6 MCM 39: Mains Filter

Frequency: 50 c/s.

Mounting: Rack. 19in x $5\frac{1}{4}$in x $3\frac{1}{2}$in

9.7 MCM 40: Control Unit

Facilities: Control and Test facilities for Engineers and Programmers.

Temperature: 0°to +55°C. (Non-derangement - 40°C to + 100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sect 1

Size: 19in rack mounting x $5\frac{1}{2}$in high x 6in deep
Weight: Approx. 20 lb.

9.9 MCM 43: Display Unit

Facilities: Displays of registers and control bistables.

Temperature: -10°C to +45°C (non-derangement, -40°C to +100°C)

Humidity: 0 - 95°RH.

Construction: Generally to DEF-133 Sect. L.1

Size: 19in Rack Mounting x $8\frac{3}{4}$in high x $7\frac{3}{4}$in deep
Weight: Approx. 18 lb.

9.10 MCM 44: Display Unit, free standing.

Desk version of MCM 43.

Size: $16\frac{5}{8}$in x $8\frac{5}{8}$in x 9.3/32in. Weight: 16 lb.

9.11 MCM 52: Marginal Test Unit

Facilities: Varies power supplies, timing, amplifier threshold etc.

Size: Held in attache case 13in x 7½in x 9in. Weight: 9¼lb

Temperature: -10 to 55°C (non-derangement, -40°C to +100°C)

Humidity: 0 - 95°RH

Construction: Generally to DEF-133 Sect. L.1

9.12 MCB 60: Paper Tape Controller

Facilities: Provides controls etc. for MCB 70 and 74

Temperature: +5° to +45°C

Humidity: 0° - 95° RH

Construction: Generally to DEF-133 Sect. L.1

Size: 19in Rack Mounting x 10½in high x 12.7in deep. Weight: 30lb

9.13 MCB 70: Paper Tape Reader

Facilities: Read, 5, 7, 8, hole P.T. at 250 ch/s.

Temperature: +5 to +40°C (non-derangement -25°C to +50°C)

Humidity: 20 - 80° RH

Construction: Generally to DEF-133 Sect. L.1

Size: 6in x 10in x 10in Weight: 17lb

9.14 MCB 74: Paper Tape Punch

Facilities: Punches 5, 7, 8 hole P.T. at 110 ch/s

Temperature: +5 to +40°C

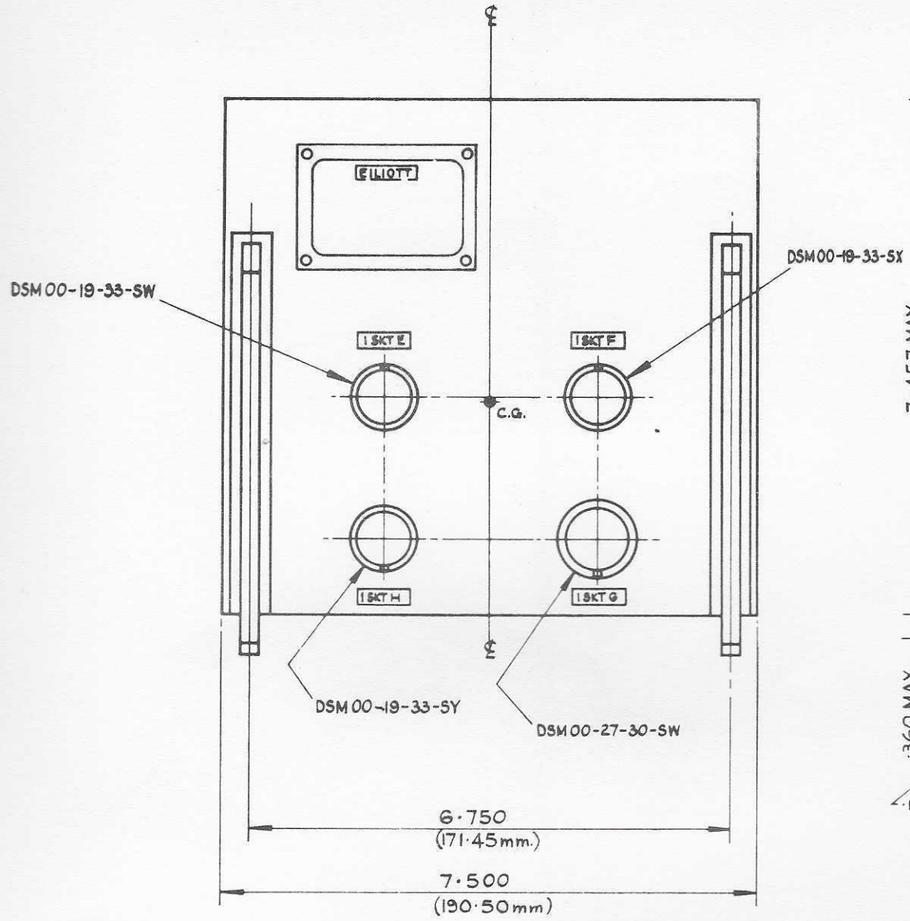
Humidity: 20 - 80°

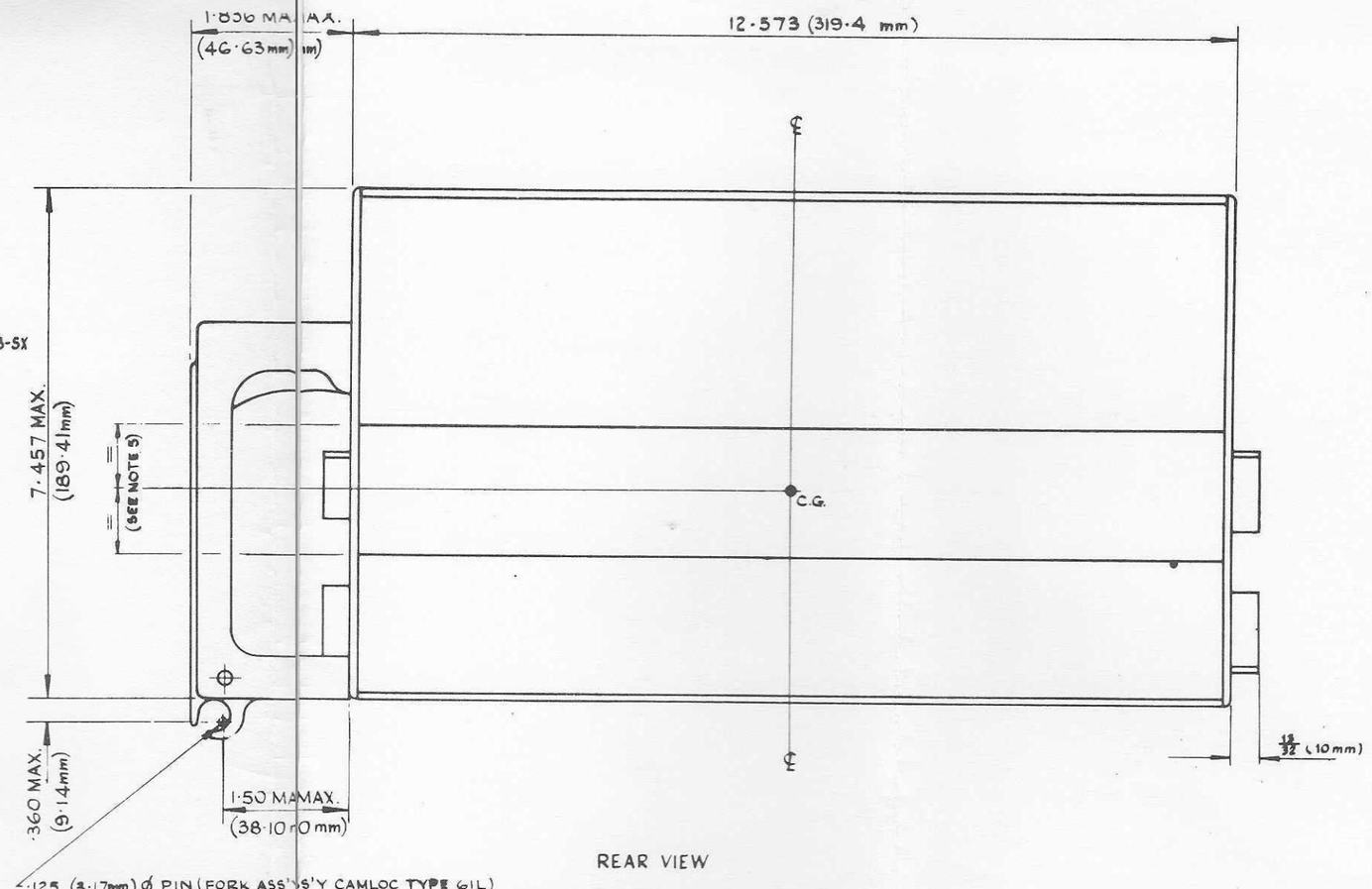
Construction: Generally to DEF-133 Sect. L.1

Size: 9½in x 11in x 16½in Weight 48lb

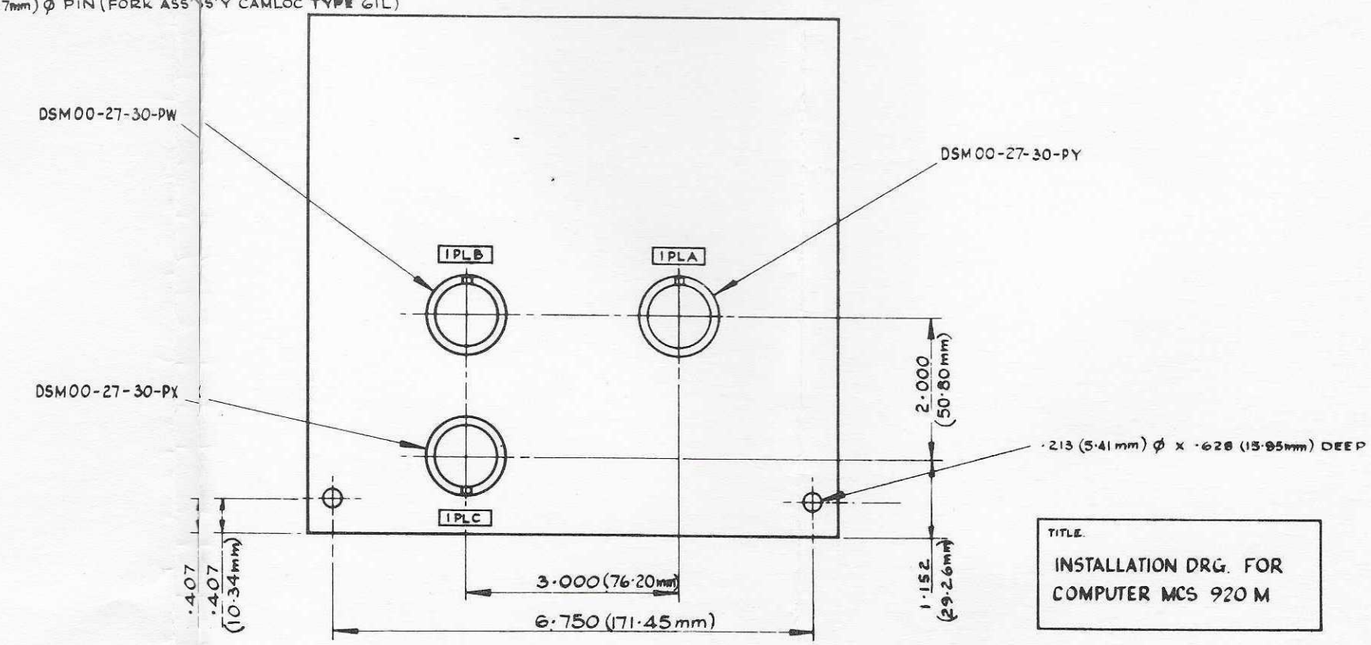
9.15 MCB 76: Paper Tape Punch

Similar to MCB 74 but punch diodes and circuitry are reversed. For use with MCB 66F only.





REAR VIEW



TITLE.
INSTALLATION DRG. FOR
COMPUTER MCS 920 M

322 D 7906

NOTES

All connectors are Hellerman Deutsch.

Total Weight = 30.10 lb. (13.7 kg).

Position of centre of gravity is estimated.

INSTALLATION DRAWING FOR COMPUTER MCS 920M Fig. 2