920M Logic Sub-Assemblies (LSAs)

Terry Froggatt, August 2023.

This document does not yet cover any of the LSAs in the Store deck.
Across the control & register decks, there are 8 columns by 56 rows of slots, of which 48 are occupied by inter-deck connectors, 9 are occupied by three 3-row LSAs, and 391 are occupied by 1-row LSAs.

The type of each 1-row LSA is marked using the resistor colour code, with three marks, of which the 1st is either a blank "-" or green "5", and with what is probably a modification number between the 2nd & 3rd mark. (Each 1-row LSA is also marked with a 5-digit code and 1 or 2 letters which probably form its unique serial number). In the descriptions below, the LSA's three colours & modification number are given in round brackets alongside the LSA type number using the abbreviations

0 Bk Black	1 Bn Brown	2 Rd Red	3 Or Orange	4 Yl Yellow
5 Gn Green	6 Bu Blue	7 Vi Violet	8 Gy Grey	9 Wt White.

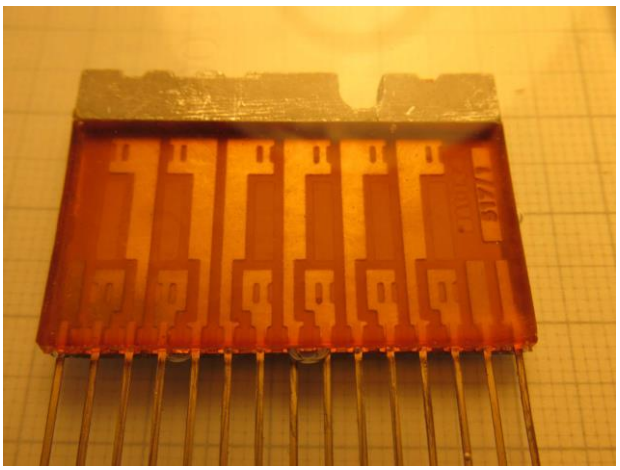
If a 1-row LSA is removed from the 920M, its contents can be seen, although it is often not possible to see much of the internal wiring. (The LSAs are best photographed like neutrinos, by dropping them into a bucket of water. When neutrinos hit water, they are travelling faster than the speed of light in water, and they cause detectable Cherenkov radiation. The Araldite surface of the LSAs is slightly rough, and the refractive index of Araldite is closer to water than to air: so putting an LSA into water hides some of the roughness at the Araldite/water boundary: the LSA can then be photographed through the smooth water/air surface. Hence the bubbles in some of the photographs). The 3-row LSAs appear to be totally enclosed in rectangular metal sleeves, preventing much examination.

The integrated circuits seen are all 930-series DTL flatpack chips, which were manufactured (at least): by Fairchild, by Texas (as seen in the photographs), and (possibly later) by Elliotts themselves. Below, I've used names of the form 9XX for the chip types and names of the form 5XX & -XX for LSA types, although as seen in some of the photographs, Elliotts used just XX for the LSA types. I have ***not*** set about removing a sample of every LSA type from the two 920Ms currently at my disposal. Although neither is working at present, both have worked in the recent past, and I do not want to risk damaging them. The information given here includes some from the LSAs that I or Dr Erik Baigar have removed in the past, but most of it has been deduced from a knowledge of the instruction set and by exploring the deck wiring. There are relatively few LSA types, most of which are used quite often, and each occurrence of a type constrains what it could be. The least well understood LSAs are those which only occur once. Anyone reading this who has more LSA photographs or other information, please do sent them to me.

For the 1-row LSAs, unless otherwise stated, pin 1 is ground and pin 15 gets power from the +5volt(logic) supply. Any LSA type containing less than 3 chips, and which has not yet been visually inspected, might also contain a decoupling capacitor between these pins. For LSAs containing just one chip, I believe that the relationship between the 14 chip pinouts and 15 LSA pinouts is always the same, with LSA pin 11 unused.

LSA type --- (-- -- -- 9)

There are 20 of these Dummy LSAs, which have to be present (in otherwise-vacant slots) to provide rigidity & heat transfer. 19 of them would be replaced by transmitters or receivers if the extra store connector PLB were fitted, and the wiring for this is all present, including +5v(logic) or +5v(store) as appropriate. The remaining Dummy LSA at A61 on the register deck has ground on pin 1 and +5v(logic) on pin 15, but is otherwise not connected. (In my coloured deck layout diagrams, the 19 transmitters and receivers are shown as if fitted, whilst all 20 dummy positions are indicated by a strike-through of their slot number).



LSA type -G? (Wide module)

This type name is not clearly readable (on several 920Ms). The only one of these is at G55-57 on the control deck. Although occupying 3 slots, only pins 2-14 of rows G55 & G56 exist, of which only 5 are used in row G56 and none are used on row G55. Pin 2 is ground, pin 14 comes from +5v(aux), and pin 12 comes from -5v(aux), this is the only use of -5v(aux) anywhere in the 920M. Only partially understood. Works in conjunction with type 504 at G52 to generate Cycle Stop (pin 13) and Reset (pin 4) signals. No adjustable resistors.

LSA type -75 (Wide module)

The only one of these is at H44-46 on the control deck. Although occupying 3 slots, only pins 2-14 of rows H45 & H46 exist. Pins H45/14 & H46/14 are ground, pin H45/02 is +5v(logic) power, and pin H46/03 receives a margins reference voltage. Only partially understood. Pin H45/03 takes the Restart input from Control Panel pin SKTG/38 and generates a short pulse on pin H45/04. The display resistors imply that this LSA houses parts of two bistables, one for Read (pins H45/07 H45/12 H46/06 H46/13) and one for Write (pins H45/06 H45/11 H45/13). Six adjustable resistors.

LSA type -76 (Wide module)

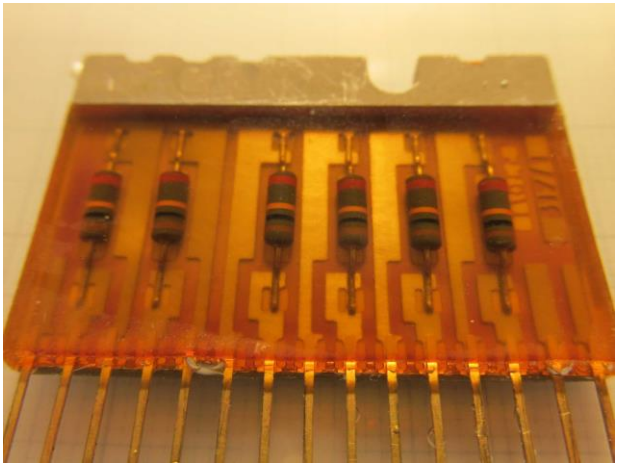
The only one of these is at H48-50 on the control deck. Although occupying 3 slots, only pins 2-14 of rows H49 & H50 exist. Pins H49/14 & H50/14 are ground, pin H49/02 is +5v(logic) power, and pin H50/03 receives a margins reference voltage. Only partially understood. This LSA appears to be responsible for generating the five main timing signals: H49/09 generates "Phase1" used to clear all of the register latches and H49/08 generates "Phase2" used to transfer data within the register latches. H49/12 generates a read-related pulse, H49/04 &/or H49/06 generates a write-related pulse, and H49/05 generates what looks like a "completed" pulse. Six adjustable resistors.

LSA type -77 (-- Vi Vi 10)

There are 2 of these, at F53 & F54 on the control deck. They provide a voltage reference, like the 920B/903's LSA 08. "Input pin 2 varies output pin 10 voltage for marginal test". Pin 1 is ground and pin 15 is +5v(logic), as normal. The other 11 pins are unused. Input PLA/18 tests wide LSA -75 using F53. Input PLA/17 tests wide LSA -76 using F54.

LSA type -78 (-- Vi Gy 7)

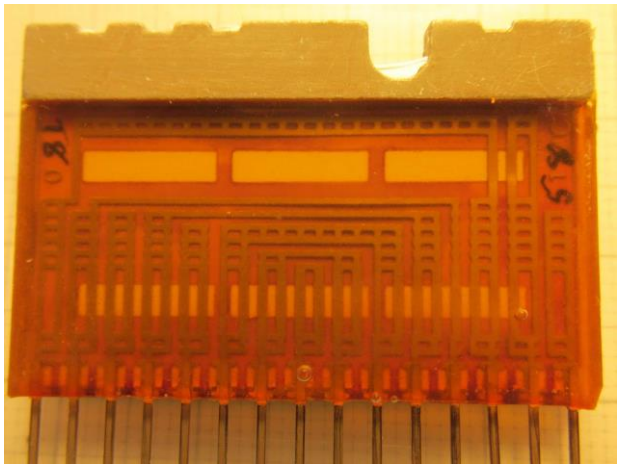
There are 18 of these: 3 on the control deck and 15 on the register deck. Each contains 6*10KΩ resistors. One resistor at A27/04&05 is unused. One is wired in series with each of the 107 display outputs on SKTE & SKTF. The resistors are wired between the following pin pairs: (02,03), (04,05), (06,07), (08,09), (10,11), (12,13). There's no consistent relationship between even-v-odd pin and source-v-display (but the display connections all occur first my WIRING database). There are no power connections: pins 1 & 15 and pin 14 are unused.



LSA type -79 (-- Vi Wt 7)

The only one of these is at G54 on the control deck. It contains 6*150Ω resistors. One resistor at G54/12&13 is unused. The other 5 are used to pull down certain Control Panel inputs. The resistors are wired between the following pin pairs: (02,03), (04,05), (06,07), (08,09), (10,11), (12,13). Consistently the even pin is the signal and the odd pin is ground. There are no power connections: pins 1 & 15 and pin 14 are unused.

LSA type -80 (-- Gy Bk 7) & LSA type -81 (-- Gy Bn 7)



The only type -80 is at A26 and the only type -81 is at A51, both on the register deck.
They both just contain links between pairs of pins:

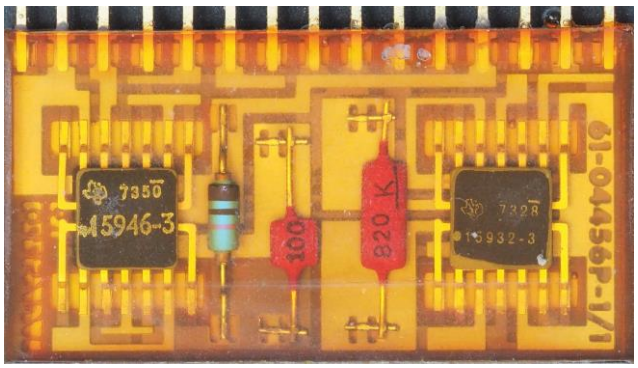
Type -80 at A26: 01=13, 02=12, 04=11, 06=10, 07=09.
Type -81 at A51: 01=14, 02=13, 03=12, 04=11, 05=10, 06=09.

They are not connected to ground or power, but unusually both use pin 1 for data. They appear within the wiring which shifts the A-register left 7 places when paper tape is read. Possibly there was some uncertainty about the shift distance when the 920M was designed, although all (earlier & later) 920s used the same 7-place shift, regardless of whether they read 7 or 8 bits from the reader. The A26/01&13 link is not actually used, and pin A26/08 is not connected in the LSA type -80 but it is connected in the deck to A51/01. These facts and the fact that the -80 and -81 are different, might offer some clues. (For example, what happens if they are swapped?)

LSA type 502 (Gn Bk Rd 4)

The only one of these is at E28 on the control deck. This appears to function identically to an LSA type 562, which provides four 2-input Nand Gates. (So what is the difference?)

LSA type 504 (Gn Bk Yl 2)



The only one of these is at G52 on the control deck. Contains 1*946 & 1*932 (with two high-fanout Buffer outputs) plus 2 capacitors & 1 resistor. The power on pin 15 comes from +5v(aux) ***not*** +5v(logic), likewise for the adjacent G53. Only partially understood. Works in conjunction with type -G? at G56 to generate Cycle Stop (pin 6) and Reset (pin 4, also 3 &/or 8) signals. Two pins take input from the Control Panel. Pin 14 is pulled down by a 150ohm resistor, and causes a Reset if pulled up by Control Panel pin SKTG/33, but this state does not latch. Pin 13 floats high, but if pulled low by SKTG/08 it inhibits the effect of pin 14. It looks as though, in the past, pin 14 did latch "Reset", and a low on pin 13 was "Jump" which cleared it, This LSA also receives a (power good?) signal on pin 7 from PLA/21, and a (temperature?) signal from the store on pin 12, and it generates a (power good?) signal to the store on pin 2. These signals also affect &/or are affected by the aforementioned Reset signals. (Photo: Dr Erik Baigar).

LSA type 509 (Gn Bk Wt 5)

The only one of these is at E47 on the control deck. In conjunction with the expanders at E46, it is used to check if the 16-bit address in the J-register is within initial instructions, namely between 8180 and 8191 inclusive. It also incorporates a latch (probably just two gates), to disable initial instructions when a program terminate (15 7168) is obeyed, by an upward Terminate pulse on pin 11; it is initially set to enabled by a downward Reset pulse on pin 13. There is no pin on E47 to display the latch's state on SKTE or SKTF.

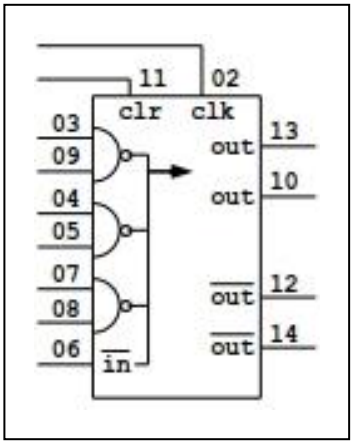
On the deck, E47 pins 2 & 7 are interconnected, but they are not connected to the rest of the deck, or to the 509 internally. This link would have been required if E47 had previously been just a generic 564 (as suggested by the pin 8 expander input) without the latch, using 1*930, whereas the bespoke 509, which is probably 2*930, implements this link internally. Terminate is connected via a long pink wire to pin 11, which the 564 would have ignored, whereas

a 564 would not have ignored the Reset connection to pin 13 which is implemented in the deck. This suggest a deck design change was made to add the Reset link, but that the Terminate link was deemed too remote. There is no suggestion that the 920Ms currently at my disposal were upgraded. They are MCM7s with no extra store socket, so fitting the latch would only release 12 store locations. The earlier MCM2 (5µsec) and MCM5 (2µsec) did have the extra store capability, and the latch would enable the gap between the stores to be removed. This implies that the design change seen in MCM7s would have been present in the MCM5 (and possibly also in the MCM2).

LSA type 551 (Gn Gn Bn 7)

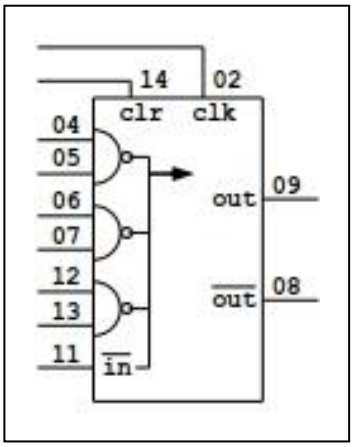
There are 60 of these one-bit two-stage latches:

53 on the register deck for the A-register(18), Q-register(18), J-register(16) and "Q00";
7 on the control deck for the C-register(6) (microprogram counter) and "A19".



This latch has an input stage and an output stage. The input stages of all 551s are cleared simultaneously by an upward pulse (which I have called "Phase1") on pin 11, then they can be set by a high on pins (3&9) or (4&5) or (7&8) or by a low on pin 6, (the setting inputs are actually present before & during the clearing pulse as well as after it). The pin 6 input is used: on the A-register for the Collate/IFU/PTS input from the Carry LSA, and on the Q-register bit 2, and on "A19". The data is transferred from the input stage to the output stage by an upward pulse on pin 2, this signal being gated elsewhere by a signal which I have called "Phase2"; each pin 2 presents two loads to the gating signal. The primary direct output is on pin 13 with its inverse on pin 12, the primary direct output is used by the Adder and by the display. A secondary direct output is on pin 10 with its inverse on pin 14, the secondary output is used for data to the IFU & PTS from the A-register, and for addresses to the internal & external stores and to the initial instructions decode, all from the J-register. The primary outputs do not emerge until it is safe to route them through the Adder back into the registers. The secondary outputs seem to emerge slightly sooner, and are used in "the sooner the better" contexts: possibly they are outputs from the input stage. Or possibly the secondary & primary outputs are generated on the leading & trailing edges respectively of the pin 2 pulse. Contains 3*946.

LSA type 552 (Gn Gn Rd 7)

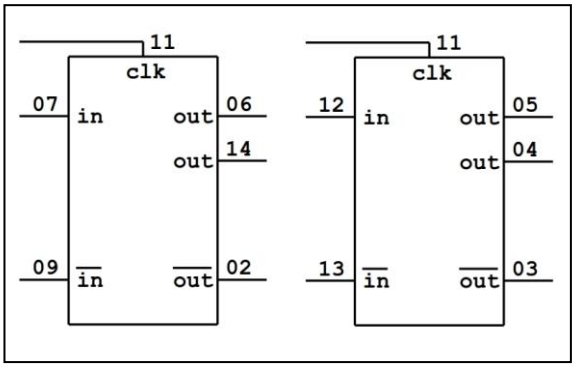


There are 18 of these one-bit two-stage latches on the register deck, all for the M-register. This latch has an input stage and an output stage. It is not clear how this LSA differs from Type 551, except that no secondary outputs are used and some pinouts are different. The input stages are cleared by the same upward pulse (which I have called "Phase1") but on pin 14, then it can be set by a high on pins (4&5) or (6&7) or (12&13) or by a low on pin 11, The pin 11 input is used for inputs from internal & external stores and is not gated: the signals are strobed within the store. The data is transferred from the input stage to the output stage by an upward pulse on pin 2, this signal being gated elsewhere by a signal which I have called "Phase2"; each pin 2 presents two loads to the gating signal. The output is on pin 9 with its inverse on pin 8; both are inputs to the Adder, and the appropriate bits of both are inputs to the P-register (peripheral address) or I-register (instruction function). The direct output also goes to the display & via an inverter to the internal store, and the inverse output also goes via an inverting transmitter to the external store. Probably 3*946 like 551.

LSA type 553 (Gn Gn Or 7)

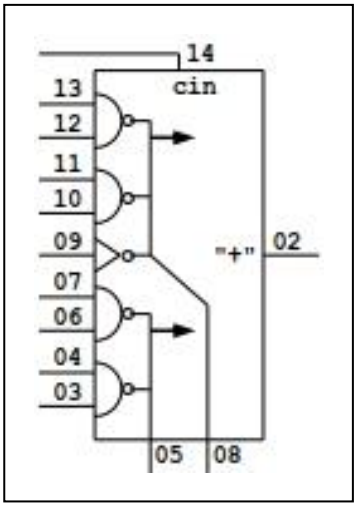
There are 10 of these two-bit latches:

1 for the 2-bit E-register (program level) on the control deck;
7 for the 13-bit P-register (peripheral address) and
2 for the 4-bit I-register (instruction function) on the register deck.



Both halves require a direct & inverse input, although these terms are interchangeable: the pinouts given here are as used by the I-register & E-register; for some bits of the M-register, direct & inverse are reversed. In each LSA, one bit uses pin 7 for the direct input & pin 9 for the inverse input, and pins 6 & 14 for direct outputs & pin 2 for the inverse output. The other bit uses pin 12 for the direct input & pin 13 for the inverse input, and pins 5 & 4 for direct outputs & pin 3 for the inverse output.

Pins 5 & 6 appear to be the primary outputs, with the display resistors moving from them to pins 14 & 4 if pins 5 & 6 are used elsewhere. Data is clocked into both bits by an upward pulse on the shared pin 11, from DtE or tP or tI respectively (all of which are gated by "Phase2"). Chips used uncertain: 930-series flip-flops could be used, but more likely the same simpler gates are used as in other LSAs. (It is not clear whether pin 11 presents one or two loads: the tI pulse drives 2 LSAs and 4 bits, the tP pulse drives 7 LSAs and 14 bits, both drivers use buffer outputs). (In my coloured deck layout diagrams, the signals to the left & right of the comma correspond to the left & right of the diagram above).

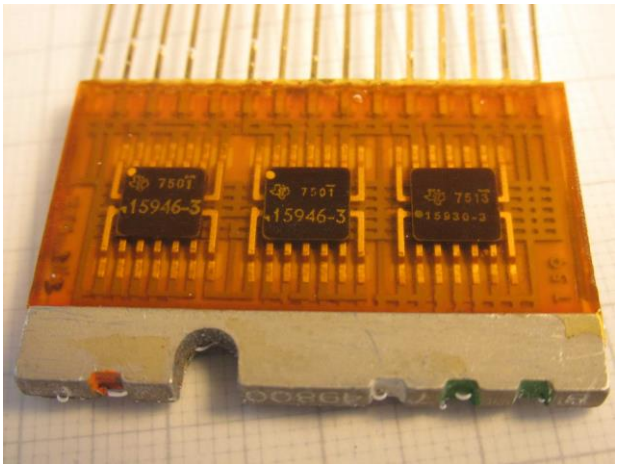


LSA type 554 (Gn Gn Yl 7)

There are 18 of these Adders on the register deck. The Adder function or its inverse is output on pin 2. The "AQDoperand" (A-register, Q-register, or D="all ones") input is taken from pins (10&11) or (12&13) or pin 9 (pin 9 is for D, the other inputs vary from bit to bit), and the inverse of this emerges on pin 8 for the Carry LSA. The "MNJoperand" (M-register, N=Minverse, or J-register) input is taken from pins (3&4) or (6&7) or not pin 5 (pin 5 is for J, the other inputs vary from bit to bit), and the inverse of this emerges on pin 5 for the Carry LSA. Yes, pin 5 is bidirectional, it is used to input "not Jreg&JtF" (from an external 567: there are too few pins to use the 554's spare gate) to a wire-ored junction in (and used by) the Adder, and to output the result to the Carry LSA. Pin 14 is carry-in or its inverse. Carry-in to bit 1 can be used to Add +1 to either operand (or both).
Carry input pin 14 and Adder output pin 2 are:

direct for bits 1 4 5 8 9 12 13 16 17, inverse for bits 2 3 6 7 10 11 14 15 18.
Uses 3*946. (See my "conjecture" diagrams).

LSA type 556 (Gn Gn Bu 7)
LSA type 557 (Gn Gn Vi 7)
LSA type 558 (Gn Gn Gy 7)
LSA type 559 (Gn Gn Wt 7) =>



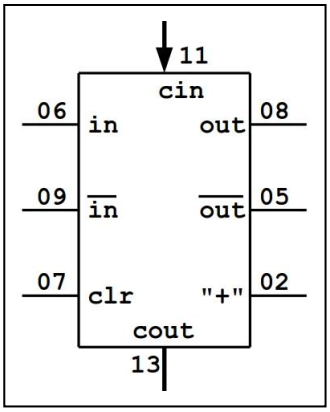
There are a total of 18 of these, all on the register deck, arranged in the following sequence:

5 of 556 at bits 1 5 9 13 17
4 of **558** at bits 2 6 10 14
4 of **557** at bits 3 7 11 15
5 of 559 at bits 4 8 12 16 18 (pictured).

They each perform two functions: they implement Carry, and they gate three further inputs into the A-register.

556 & 557 perform a simple carry, using the two adder inputs of the current bit, and the carry-out from the previous bit. 558 & 559 perform a lookahead carry, using the two adder inputs of the current bit, and the two adder inputs to the previous bit, and the carry-in to the previous bit, namely the carry-out from two bits earlier. Thus only ***one*** gate delay involved in propagating the carry through ***two*** bits. But as a consequence, the sense of the carry inverts every two bits, so the simple & lookahead Carry LSAs each requires two flavours. Also nine bits of the Adder function output need an inverter. (Why not two flavours of Adder? I think there is a spare gate). The 4-type LSA cycle changes for bit 18, where a 559 is used (rather than a 558) so that the carry-out is replaced by the 19th Adder bit (F19) needed for right shifts and multiply, (not to be confused with the 18th Adder output, latched into LSA F42 for divide, which I've called A19).

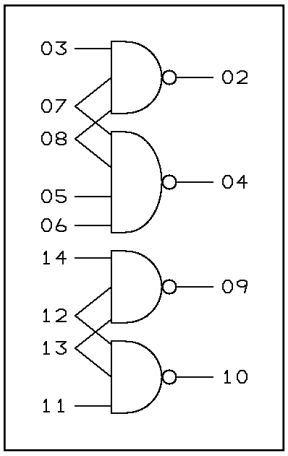
All four Carry LSA types also gate three further inputs into the A-register: Collate (available for the carry calculation), and data from the IFU and from the PTS. Irritatingly not only does the relationship between signals & pins switch around like inputs to the Adder & the register latches, the four flavours actually use different input and output pins (seemingly unnecessarily).Type 559 uses 2*946 & 1*930, type 588 probably uses the same, and types 556 & 557 probably each use just 2*946. (For all four flavours, see my "conjecture" diagrams).



LSA type 560 (Gn Bu Bk 7) =>

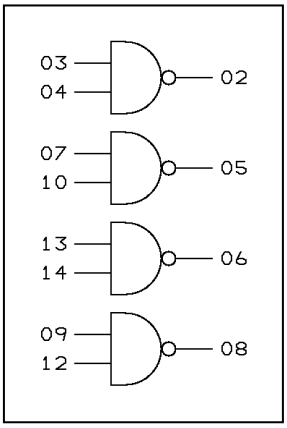
There are 6 of these, all on the control deck, each alongside a 551 one-bit latch. Together, each pair implements one bit of the 6-bit microprogram Counter. All type 551 LSAs are cleared by the Phase1 pulse, including the 6 here, so the type 560 LSA must

be latching the counter value at that point, hence the reset input on pin 7 to initially clear the latches. The 560 chain normally Adds +1 to the Counter value: using the old counter value (from 551 pin 13 into 560 pin 6), and its inverse (from 551 pin 12 into 560 pin 9), the new counter value is returned (from 560 pin 2 into 551 pin 8, where it is gated in by "don't clear C1 to C6" on pin 7). Carry-in is on pin 11; normally +1 is fed into the least-significant bit, but this can be suppressed by the SUPPRESSCOUNT microprogram waveform, or by Cycle Stop from the Control Panel; carry-out is on pin 13. The Counter value (old or new?) is output for decoding into the microprogram, from the 560 pin 8 with its inverse on pin 5. The microprogram also uses output from the most-significant 551 (CtA6). Apart from the reset, there are no clocking pulses into a 560. Chips used uncertain.



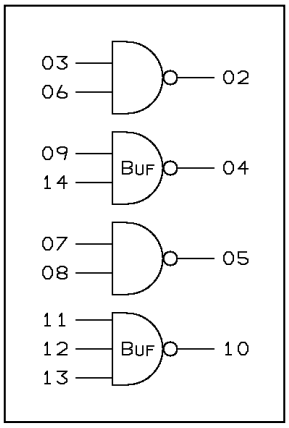
LSA type 561 (Gn Bu Bn 7) =>

There are 19 of these Decoders, all on the control deck. Each provides three 3-input Nand Gates and one 4-input Nand Gate, probably using 2*930, with some shared inputs to fit into 15 pins overall. Mainly used to decode the inputs to the microprogram. The 4-input gate is sometimes used to add a conditional test, for example the 3-input G16/02 decodes "Function 7 step 9", and the 4-input G16/04 decodes "Function 7 step 9 and A18=1", using 2 inputs shared internally and a 3rd input shared externally.



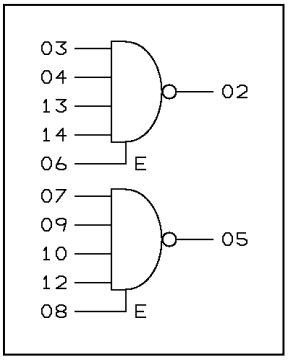
<= LSA type 562 (Gn Bu Rd 10)

There are 27 of these, all on the control deck.
Each provides four 2-input Nand Gates using 1*946, and a capacitor. Pin 11 is unused.



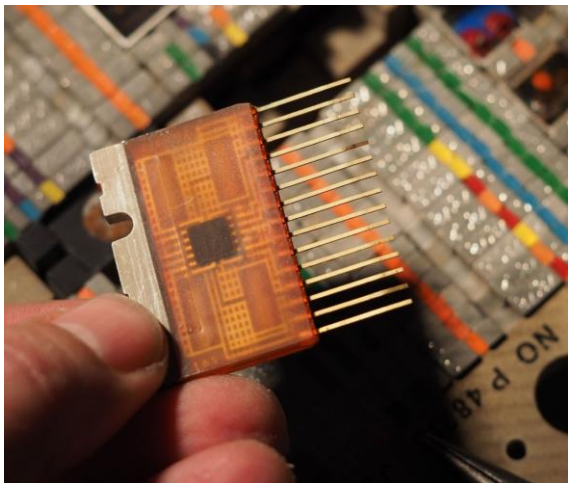
LSA type 563 (Gn Bu Or 7) =>

There are 13 of these, all on the control deck. Each provides two 2-input Nand Gates probably using 1*930, and one 2-input & one 3-input high-fanout Nand Buffer probably using 1*932. The power on G53/15 comes from +5v(aux) ***not*** +5v(logic).



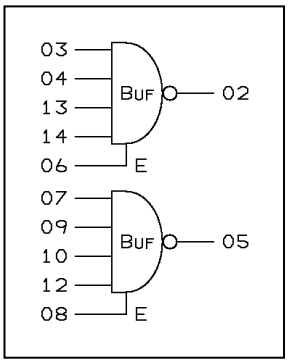
LSA type 564 (Gn Bu Yl 7) =>

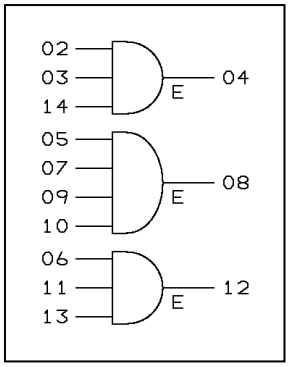
There are 40 of these, all on the control deck.
Each provides two 4-input expandable Nand Gates, using 1*930. Pin 11 is unused.



<= LSA type 565 (Gn Bu Gn 7) =>

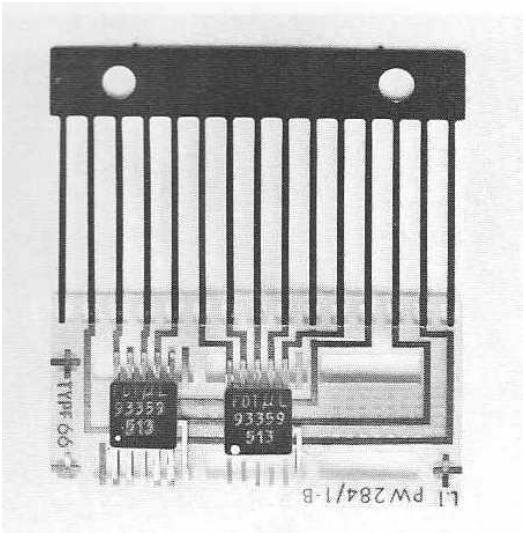
There are 14 of these, all on the control deck. Each provides two 4-input expandable high-fanout Nand Buffers, using 1*932. Pin 11 is unused. (Photo: Dr Erik Baigar).





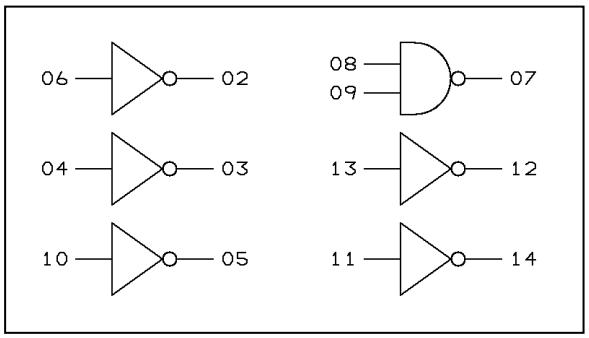
<= LSA type 566 (Gn Bu Bu 7) =>

There are 13 of these, all on the control deck. The Elliott sales brochure photograph shows one during construction. Each provides one 4-input & two 3-input Expanders, using 2*933. There are no power connections: pins 1 & 15 are not connected on the deck, although the DTL manufacturer's literature shows some diodes internally wired to the 933 ground pins. The highest number of inputs seen on any gate is 14: four on a 564 or 565 plus all 10 inputs of one 566.



LSA type 567 (Gn Bu Vi 8)

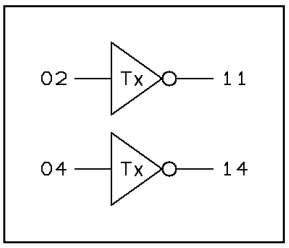
There are 39 of these, 12 on the control deck and 27 on the register deck. Each provides five Inverters and one 2-input Nand Gate, using 1*930 and 1*946 (providing exactly 6 outputs) and a capacitor. In 16 of these LSAs on the register deck, the Nand Gate is used to gate the J-register into the Adder. (In my coloured register deck layout diagram, these are shown as "Jgate+5inv" rather than "Nand+5inv").



LSA type 573 (Gn Vi Or 8)

There are 24 of these fitted and 18 more are added for extra store, making 25 on the control deck and 17 on the register deck. Each provides two similar inverting transmitters, used for data, address and control signals. to PLB (extra store), PLC (IFU), and SKTH (PTS). The power on pin 15 comes from +5v(store) ***not*** +5v(logic). Contains 1*946 plus a dual transistor & 4 resistors. (In my coloured deck layout diagrams,

the signal left of the comma relates to pin 2 input & pin 11 output,
the signal right of the comma relates to pin 4 input & pin 14 output).

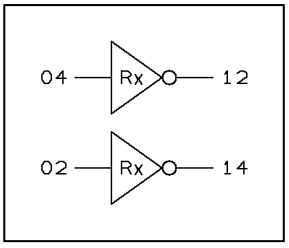


LSA type 585 (Gn Gy Gn 8)

There are 18 of these on the register deck. Each provides two inverting receivers, which may well differ from one another, and where logically at least one of them must differ from those in LSA type 587. Consistently, suggesting there is a difference,

input pin 2 output pin 14 receives a data bit from PLC (IFU). and
input pin 4 output pin 12 receives a data bit from PLB (extra store)

So the extra store data receivers are present even when PLB is not.



LSA type 587 (Gn Gy Vi 8)

There are 8 of these fitted and 1 more is added for extra store, all on the control deck. Each provides two similar inverting receivers, used for data from SKTH (PTS), and control signals from PLB (extra store), PLC (IFU), and SKTH (PTS).
(In my coloured deck layout diagrams, for LSA 585 & 587,

the signal left of the comma relates to pin 2 input & pin 14 output,
the signal right of the comma relates to pin 4 input & pin 12 output).